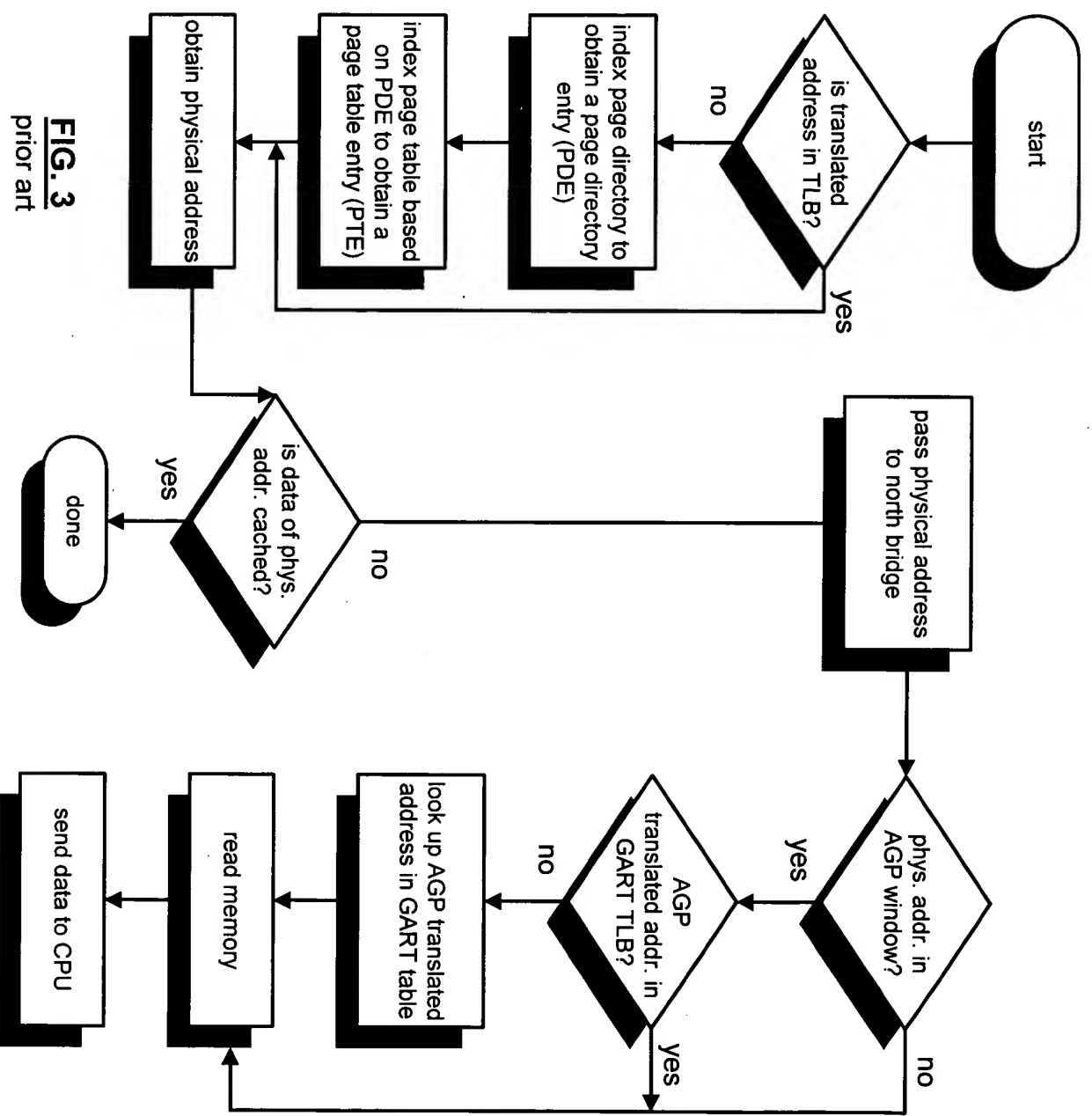
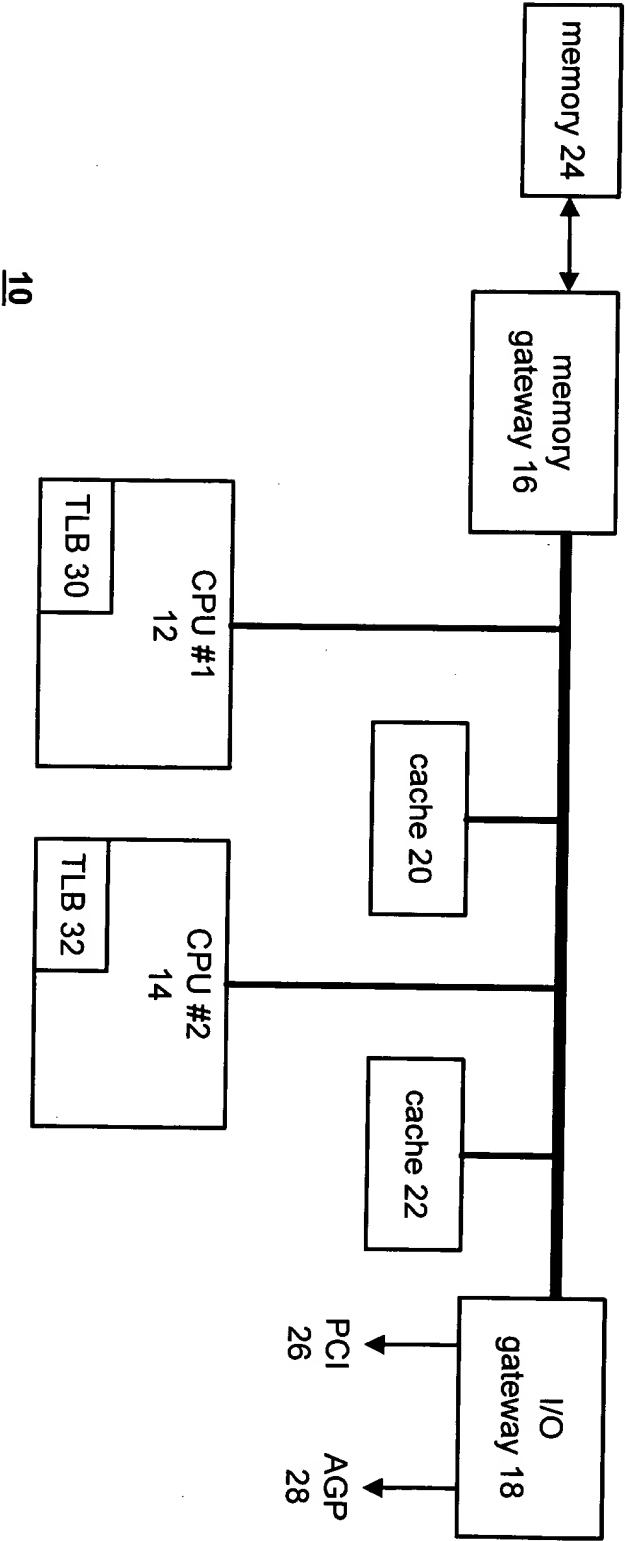


FIG. 1 and FIG. 2 are prior art diagrams showing a system architecture and its mapping between virtual and physical address spaces.

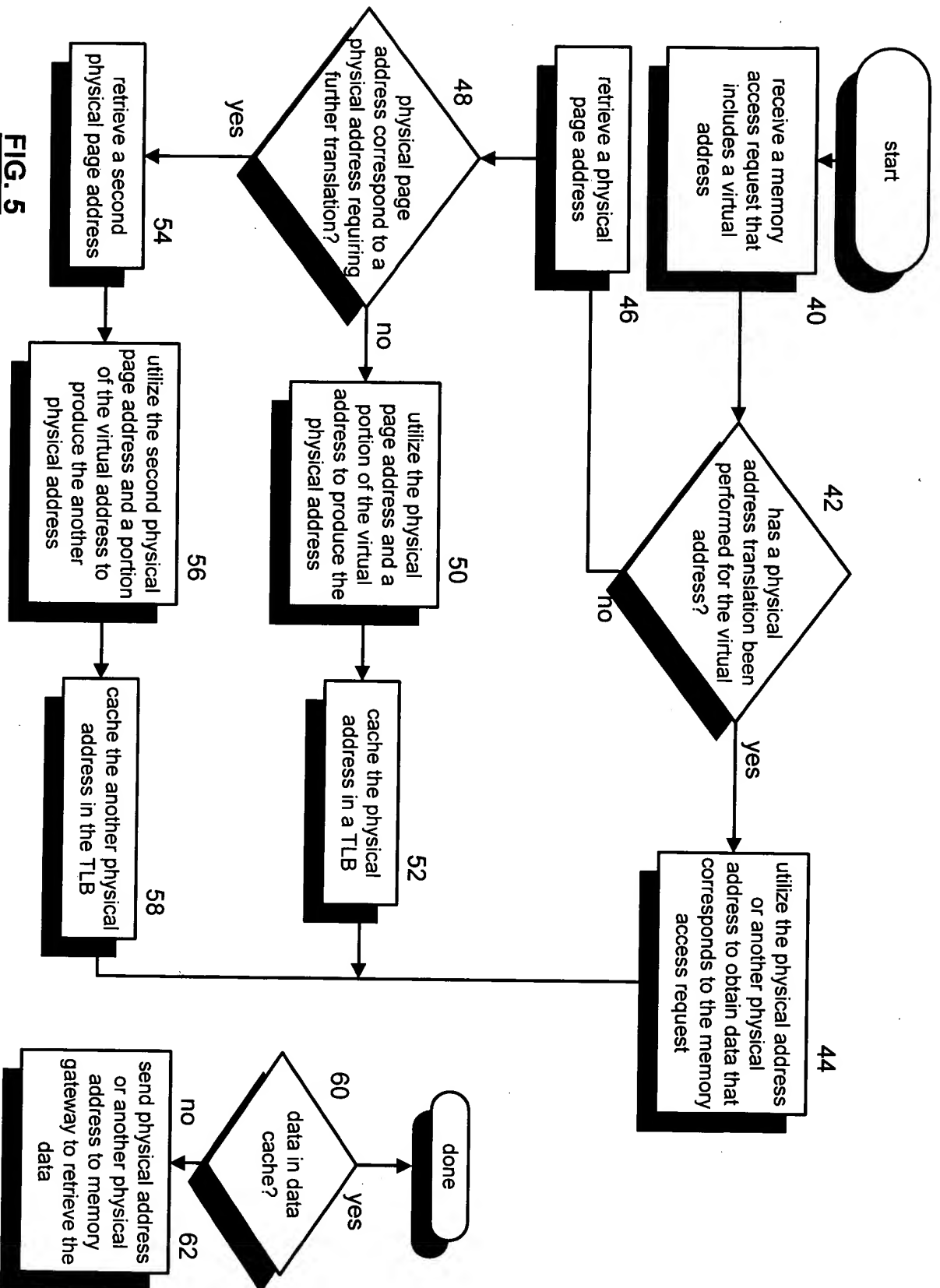


**FIG. 3**  
prior art

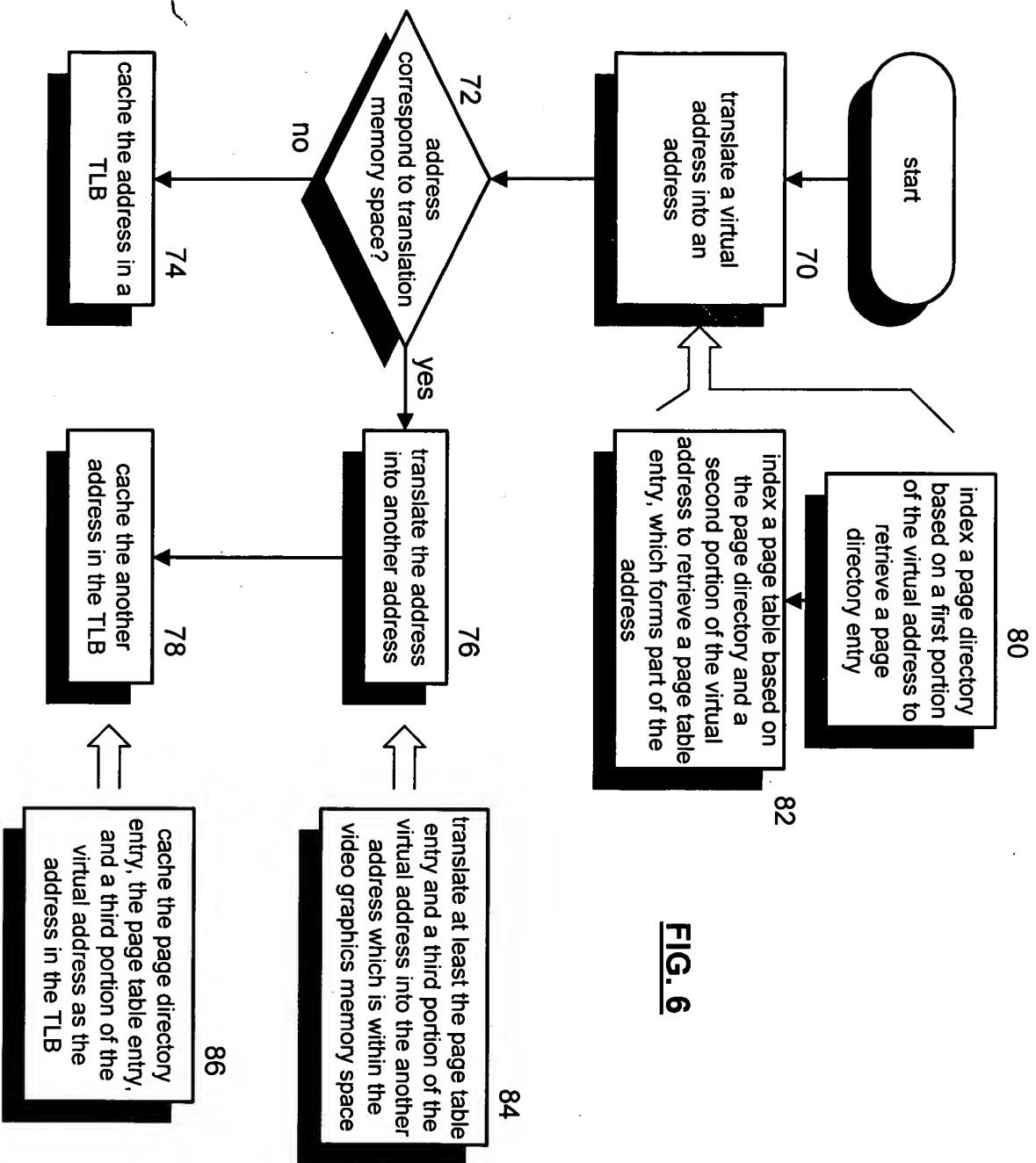
FIG. 3 is a flowchart illustrating a process for address translation and data retrieval. The process starts at a terminal 'start' and proceeds to a decision diamond 'is translated address in TLB?'. If the answer is 'yes', the process proceeds to 'pass physical address to north bridge'. If 'no', it goes to 'index page directory to obtain a page directory entry (PDE)', then to 'index page table based on PDE to obtain a page table entry (PTE)', and then to 'obtain physical address'. From 'obtain physical address', the flow enters another decision diamond 'is data of phys. addr. cached?'. If 'yes', it reaches a 'done' terminal. If 'no', it enters a decision diamond 'phys. addr. in AGP window?'. If 'yes', it proceeds to 'AGP translated addr. in GART TLB?'. If 'no', it goes directly to 'read memory'. From 'AGP translated addr. in GART TLB?', if 'yes', it proceeds to 'read memory'; if 'no', it goes to 'look up AGP translated address in GART table', which then leads to 'read memory'. Finally, 'read memory' leads to 'send data to CPU'.



**FIG. 4**



**FIG. 5**



**FIG. 6**